Amendments to the Claims:

Please cancel claims 1-2 and 12 without prejudice as indicated below. This listing of claims will replace all prior versions and listing of claims in the application:

Listing of Claims:

1-3. (Canceled)

4. (Previously presented) An input buffer circuit having an input and a buffer output, said input buffer operable in a normal mode and a hot-plug mode, comprising:

a pull-up path coupled between a first circuit supply and the buffer output;

a pull-down path coupled between the buffer output and a ground reference voltage;

a first transistor coupled between the input and the pull-up path to activate the pull-up path;

a second transistor coupled between the input and the pull-down path to activate the pull-down path; and

a third transistor for protecting the pull-up path from over-voltage;

wherein the input buffer circuit is configured to prevent an over-voltage condition on each of the plurality of transistors and the input buffer circuit is configured to allow a hot-plug operation.

5. (Canceled)

6. (Previously presented) An input buffer circuit having an input and a buffer output, said input buffer operable in a normal mode and a hot-plug mode, comprising:

a pull-up path coupled between a first circuit supply and the buffer output;

a pull-down path coupled between the buffer output and a ground reference voltage;

a first transistor coupled between the input and the pull-up path to activate the pull-up path;

a second transistor coupled between the input and the pull-down path to activate the pull-down path; and

a third transistor for protecting the pull-up path from over-voltage

wherein the pull-up path includes:

a first reference voltage; and

a first pair of transistors including a first and second pull-up transistor coupled in series, said first pull-up transistor having a gate coupled with the first transistor and said gate biased by the third transistor and said second pull-up transistor having a gate biased by the first reference voltage.

7. (Original) The input buffer circuit of claim 6, wherein the pull-down path includes:

a second reference voltage; and

a second pair of transistors including a first and second pull-down transistor coupled in series, said first pull-down transistor having a gate coupled with the second transistor and said second pull-down transistor having a gate biased by the second reference voltage.

8. (Original) The input buffer circuit of claim 7, wherein the first reference voltage is approximately 1.0 volts, and the second reference voltage is approximately 2.5 volts.

9. (Original) The input buffer circuit of claim 4, further comprising:

a first bias voltage for biasing the first transistor; and

a second bias voltage for biasing the second transistor.

10. (Previously presented) An input buffer circuit having an input and a buffer output, said input buffer operable in a normal mode and a hot-plug mode, comprising:

a pull-up path coupled between a first circuit supply and the buffer output;

a pull-down path coupled between the buffer output and a ground reference voltage;

a first transistor coupled between the input and the pull-up path to activate the pull-up path;

a second transistor coupled between the input and the pull-down path to activate the pull-down path;

a third transistor for protecting the pull-up path from over-voltage;

a first bias voltage for biasing the first transistor; and

a second bias voltage for biasing the second transistor;

wherein the first bias voltage is approximately 1.0 volts during the normal mode and is approximately the input minus two diode drops during the hot-plug mode.

11. (Previously presented) An input buffer circuit having an input and a buffer output, said input buffer operable in a normal mode and a hot-plug mode, comprising:

a pull-up path coupled between a first circuit supply and the buffer output;

a pull-down path coupled between the buffer output and a ground reference voltage;

a first transistor coupled between the input and the pull-up path to activate the pull-up path;

a second transistor coupled between the input and the pull-down path to activate the pull-down path;

a third transistor for protecting the pull-up path from over-voltage;

a first bias voltage for biasing the first transistor; and

a second bias voltage for biasing the second transistor;

wherein the second bias voltage is approximately 2.5 volts during the normal mode and is approximately the input minus two diode drops during the hot-plug mode.

12. (Canceled)